It's time to rethink…

Advanced process dummy fill

STATE OF THE ART

Redesigned engine optimizes fill methodologies for the most advanced processes, including dual- and quad-patterning.

FLEXIBILITY

Advanced features support process- and design-based constraints and optimize fill for all designs, from digital processors down to 10nm to 1µ bipolar devices. DRC compatible by design.

PRODUCTIVITY

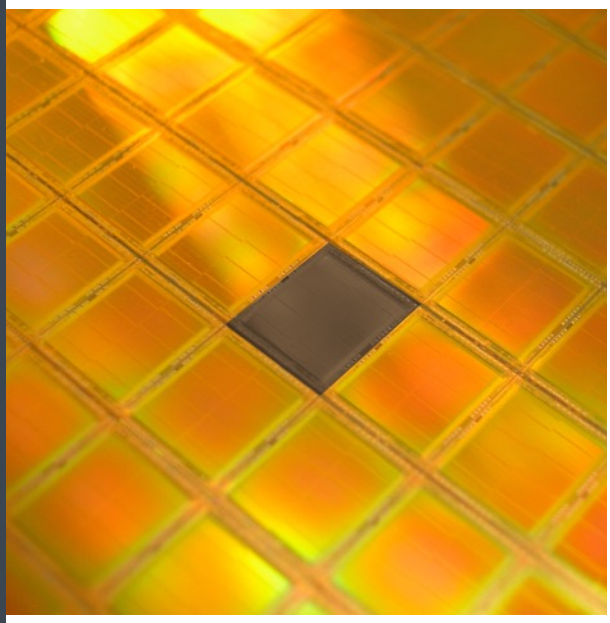
For the most demanding designs, GOTstyle offers a parallel mode, which splits dummy insertion between different processors, dramatically speeding up calculation while reducing memory usage.

RELIABILITY

Dummy fill solution has been used in production by leading companies for years.

PORTABILITY

GOT style supports standard layout formats: GDSII, OASIS, OASIS.MASK.



- Advanced insertion algorithm with minimal result file size
- Parasitic effect minimization
- Support for advanced nodes, 14nm and below
- Complex dummy tiles instantiation
- Tile interconnection
- Staged insertion for complex fill operations and high performance parallelization

Shrinking geometries, new manufacturing paradigms, exploding file sizes… It's time to rethink everything.

XYALIS increases the productivity, reliability, and capability of dummy fill with GOTstyle, a redesigned fill engine that handles the largest designs with maximum performance and minimum memory requirements thanks to the new GDSII & OASIS (GOT) data representation engine tailored to leverage native OASIS.MASK optimizations.

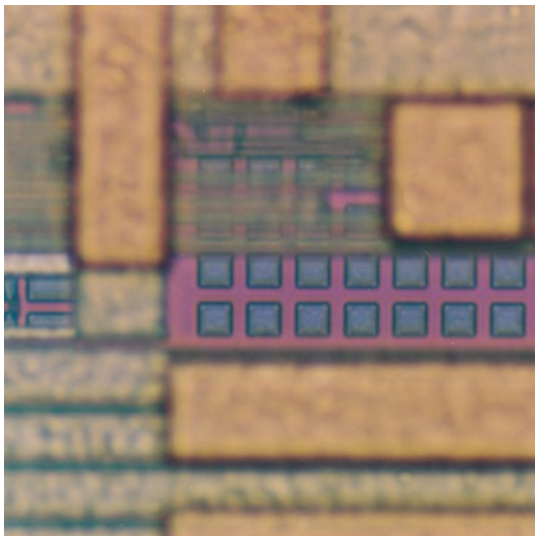
To increase manufacturing yield, designers must ensure a uniform pattern repartition over chips and wafers. Dummy tiles must be inserted in low-density design areas, to help flatten the surface of each metal layer before CMP. These additional polygons, though electrically inactive, may cause parasitic effects that must be minimized and taken into account early in the design process to avoid behavioral and timing issues.

GOTstyle redesigned fill engine optimizes new fill methodologies required for the most advanced processes, including dual- and quad-patterning. GOTstyle maximizes CMP yield with a highly accurate patented tile insertion algorithm based on local density and roughness calculations and their variations over large areas.

GOTstyle minimizes parasitic effects by limiting the number of dummy structures and positioning them away from active geometries. Balancing dummy tile insertion around critical nets allows for precise control of impact on timing.

XYALIS

Features and Benefits



- **Advanced insertion algorithm with minimal result file size**
  GOTstyle patented insertion algorithm combines global topology requirements with local design rules to instantiate dummy tiles. A topology analyzer calculates local density and roughness while a gradient analyzer minimizes local variations that negatively impact yield, taking into account scribe density at the edge of the chip. GOTstyle inserts a minimum number of tiles and generates a small DRC-compliant result file.

- **Parasitic effect minimization**
  Advanced features such as the Keep Away function that increases space between inserted dummy tiles and critical nets and non orthogonal insertion grid for better net balancing minimize parasitics generated by dummy fill and avoid parasitics variations along the design grid.

- **Support for advanced nodes, 14nm and below**
  GOTstyle grid-based insertion combined with adjustable alignment grids and automatic cuts of dummy lines enables horizontal and vertical alignment of dummies and slots for simpler mask manufacturing in case of dual- and quad-patterning.

- **Complex dummy tiles instantiation**
  GOTstyle inserts any type of dummy tiles, whatever their complexity: full-layers, regular tiles, post-OPC cells, diodes for grounding to bulk. To better control density over the different areas of the design, the insertion algorithm calculates the optimum tile size and merges dummy tiles into larger blocks if necessary.

- **Tile interconnection**
  GOTstyle offers the possibility to replace floating capacitance of disconnected dummy tiles with efficient shielding by inserting interconnection cells between contiguous dummy tiles. Interconnection cells may be defined horizontally and vertically, making it possible to stack dummy tiles through layers and to build dummy stripes within a layer.

- **Staged insertion for complex fill operations and high performance parallelization**
  By staging dependencies between different layer fill operations GOTstyle handles complex dummy fill generation with reduced computing and memory footprints. Stages insertion is also used to distribute multi-layer fill across many cores in order to dramatically speed up calculation.

ESSENTIAL COMPANION TOOLBOX

XYALIS offers a set of tools dedicated to layout manipulation that can process the largest GDSII and OASIS database, with the highest processing speed and lowest memory requirement, and provide a safe transfer to silicon for the most complex SOC designs.

SYSTEM REQUIREMENTS

Runs on any Linux workstation with RedHat 6 or above. Management of multi-cores is automatic.
A Mac OSX version is also available.
Binaries for other platforms may be provided on request.

INFORMATION

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