

IC Layout finishing software

Automated Frame Generation

REUSABILITY

A frame description file is specified per process and can be further parameterized to handle revisions and options.

SECURITY

Checks are performed at each step of the frame generation flow ensuring error free database and mask order.

RELIABILITY

XYALIS frame generation solution has been used in production by leading edge semiconductor companies for several years.

AUTOMATION

XYALIS GTframe is fully integrated in XYALIS Mask Data Preparation solution and can be scripted to run smoothly without human intervention in production mode.

PORTABILITY

XYALIS GTframe supports standard layout and job deck formats: GDSII, OASIS, MEBES.



- Reusable frame description file
- Reticule optimization
- Graphical constraint input
- Support for multi-chip assemblies
- Mask manufacturability verification
- Automatic documentation and database merging
- Essential companion toolbox

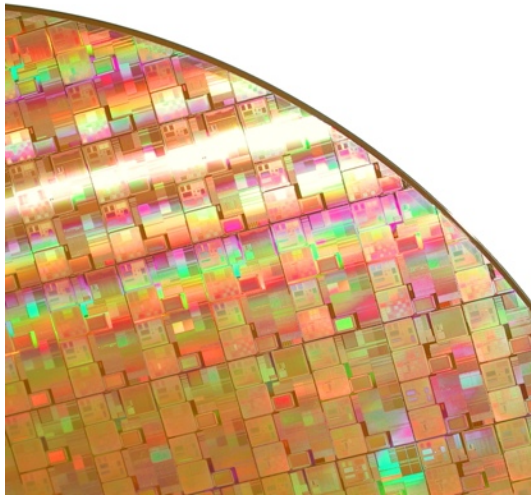
As the cost of a complete mask set has dramatically increased and now represents a significant part of the overall project cost, it is critical for design teams, mask data preparation teams, and mask shops to implement a robust and repeatable Mask Data Preparation flow, which increases the productivity of the mask set creation and removes any risk of error.

XYALIS GTframe is a frame generation solution, which automates the insertion of all process and mask specific items: alignment marks, test structures, barcodes... in the scribe lines. A reusable process specific file describes all items required by the current technology and manufacturing and inspection equipment, along with their placement constraints. The placement engine finds an optimal solution meeting the constraints while minimizing the scribe line width.

By automating a repetitive and error prone process XYALIS GTframe increases productivity by automating reticule edition and enabling maximum reuse of item definition and constraints, avoids costly errors due to manual operations, and maximizes silicon by proposing an optimum reticule placement for arrays of chips. XYALIS automatic frame generation works for both regular arrays of dies and multi-chip assemblies.



Features and Benefits



ESSENTIAL COMPANION TOOLBOX

XYALIS offers a set of software dedicated to large layout database manipulation and update that can process even the largest GDSII and OASIS database, with the highest processing speed available, to provide a safe transfer to silicon from the most complex SOC designs, recommended in every tape-out sign-off flow.

SYSTEM REQUIREMENTS

Software runs on any Linux workstation with RedHat 5 or above. Management of multi-cores or multi CPU is automatic. A MacOSX version is also available. Binaries for other platforms may be provided upon request.

INFORMATION

For more information on any of our products or services please visit us on the Web at: www.xyalis.com or mail to: sales@xyalis.com

- **Reusable process specific frame description file**

A reusable intuitive frame description file describes the process specific items and their associated constraints: location, transformation, placement order, and advanced conditional constraints. The human readable frame description file handles any type of frames and can be parameterized for reusability.

- **Reticule optimization**

XYALIS GTframe rotates the chip in order to increase the number of dies in the frame. If the mandatory items cannot be placed in the initial reticule, GTframe computes the minimum scribe line expansion necessary to place all items.

- **Graphical constraint input**

The process frame description file is a human readable intuitive description of the process specific constraints. It is easily created with any text editor or through a set of forms provided by a dedicated graphical user interface to speed up ramp-up time.

- **Support for multi-chip assemblies**

XYALIS GTframe inserts process specific items in the scribe lines of regular arrays of dies. It is also designed to insert process specific items around and in between the chips of a multi-chip assembly created with XYALIS Mask Data Preparation Solution multi-chip assembly editor.

- **Mask manufacturability verification**

A design database analyzer combined with an assembly rule checker warrants that the frame is free from error and can be manufactured. Special checks are carried out to ensure that the final mask set database can be handled with no problem by mask shop and manufacturing processing and inspection tools.

- **Automatic documentation and database merging**

User documentation is generated by the click of a button. Format and available information are customized through a plug-in mechanism. Final layout data is generated as a single database or multiple databases that can be adjusted to offer the best trade-off between job deck complexity and file size.



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